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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/543,097	07/22/2005	Keiichi Kurashina	2005_1121A	5697
513 7590 09/02/2010 WENDEROTH, LIND & PONACK, L.L.P. 1030 15th Street, N.W., Suite 400 East Washington, DC 20005-1503				
EXAMINER				
LEADER, WILLIAM T				
ART UNIT		PAPER NUMBER		
1795				
NOTIFICATION DATE		DELIVERY MODE		
09/02/2010		ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ddalecki@wenderoth.com

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Office Action Summary

Application No.

10/543,097

Applicant(s)

KURASHINA ET AL.

Examiner

WILLIAM T. LEADER

Art Unit

1795

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 June 2010.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 34, 35, 37-42, 44 and 58 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 34, 35, 37-42, 44 and 58 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB06)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. Receipt of the papers filed on June 22, 2010, is acknowledged.

Inventorship

2. In view of the papers filed January 22, 2010, it has been found that this nonprovisional application, as filed, through error and without deceptive intent, improperly set forth the inventorship, and accordingly, this application has been corrected in compliance with 37 CFR 1.48(a). The inventorship of this application has been changed by adding the following individuals as inventors: Laertis Economikos, Hariklia Deligianni, Panayotis Andricacos (deceased), John Cotte, and Keith Kwietniak.

The application will be forwarded to the Office of Initial Patent Examination (OIPE) for issuance of a corrected filing receipt, and correction of Office records to reflect the inventorship as corrected.

Specification

3. The substitute specification filed June 22, 2010, has been entered.
4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

5. Claims 34, 35, 37-39, 41, 43, 44 and 58 are rejected under 35 U.S.C. 102(c) as being anticipated by Economikos et al (US 6,773,570) for the reasons of record and in view of the following comments.

6. Applicant has amended claim 34 to recite that “the plating is performed while a change of state of the plating voltage that is applied between the seed layer and the anode occurs that results from intermittence of the plating voltage.” A dictionary definition for “intermittent” is “stopping and starting at intervals” (The American Heritage Dictionary of the English Language, New College Edition). Thus, the change of state of plating voltage that results from intermittence of the plating voltage is interpreted to mean that the plating voltage is started and stopped at intervals. Consequently, the limitation “plating is performed while a change of state of the plating voltage that is applied between the seed layer and anode occurs” is considered to refer to a plating process which includes at least one interval when plating current is applied and at least one interval when plating current is not applied. This claim limitation is considered to be met by Economikos. As shown in figure 6 and described at column 2, lines 65-67 of Economikos, electroplating and electroetching may be alternately performed a number of times. In electroplating a plating voltage is applied. In electroetching, a plating voltage is not applied. Economikos additionally discloses that during electroplating, a first amount of mechanical force is applied on the substrate against the pad (column 2, lines 57-61). During electroetching, the downward force on the wafer is reduced to allow a space greater than the boundary layer thickness to be formed (column 5, lines 8-12). This disclosure meets the limitation requiring a change of pressing state that is correlated with the change of state of plating voltage.

7. With respect to claim 37 as amended, as alternate cycles of electroplating and electroetching in the process of Economikos are performed, a pressure is increased relative to a previous pressure when applying the plating voltage, and the pressure is lowered relative to a previous pressure when not applying the plating voltage.

8. Claim 41 as amended includes the steps of plating the substrate by flowing a current between the seed layer and the anode while filling a plating solution between the seed layer and the anode and pressing the porous member against the seed layer under a pressure; after plating, stopping the flowing current and then refreshing the plating solution between the seed layer and the anode after separating the porous member from the seed layer; and repeating these steps. Economikos discloses that the plating solution is continuously dispensed on the pad while the wafer rotates with respect to the pad. The supply of plating solution to the wafer is thus constantly refreshed (column 4, lines 16-20). The limitations recited in claim 41 are met by Economikos. Since the plating solution is continuously dispensed, it is refreshed after the application of electroplating current is stopped and the pressure applied during electroplating is reduced and the pad separated by a space greater than the boundary layer thickness. As noted previously, Economikos discloses that the sequence of electroplating and electroetching may be repeated.

9. Claim 44 as amended includes the step of filling the plating solution between the seed layer and the anode; removing the plating solution existing in the gap between the porous member and the seed layer by rotating the substrate and the porous member relative to each other while pressing the porous member against the seed layer under pressure; and plating by flowing current while pressing the porous member against the seed layer under pressure. Applicant's

specification discloses that the plating solution existing in the gap between the porous member and the surface to be plated can be removed outwardly by a centrifugal force generated by the rotation of the substrate (page 15, lines 1-7). As noted above, Economikos discloses that the plating solution is continuously dispensed on the pad while the wafer rotates with respect to the pad. This would remove the plating solution in the same way it is removed in applicant's process.

10. With respect to claim 58, Economikos discloses that the sequence of electroplating and electroetching may be repeated.

Claim Rejections - 35 USC § 103

11. Claims 34, 35, 37-39, 41, 43, 44 and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Economikos et al (US 6,773,570) in view of Chadda (US 7,025,860) or Emesh et al (2002/0108861).

12. Economikos is interpreted and applied as above. As previously indicated Economikos utilizes polishing pad 20 (column 3, lines 63-65) in the process of electroplating onto the seed layer of a semiconductor workpiece. While one of ordinary skill in the art would recognize that polishing pads have a degree of porosity, Economikos does not explicitly state that the polishing pad is porous. If Economikos is interpreted as not disclosing a porous polishing pad, the use of a porous pad would have been obvious in view of Chadda or Emesh.

13. The Chadda patent is directed to a process for the electrochemical deposition and removal of a material on a workpiece surface. See the title and abstract. The workpiece may be a semiconductor wafer (column 1, lines 8-10). Chadda discloses that polishing pads may be

made of blown urethane, which contains a large number of voids, or other material such as fiber meshes or felts which are porous (column 3, lines 28-40).

14. The Emesh patent is directed to a method for electrochemical treatment of a workpiece such as a semiconductor wafer (abstract; paragraph [0002]). As shown in figure 4, wafer 60 which has a metallized surface 80 is urged against polishing pad 40 by wafer carrier assembly 130 (paragraph [0035]). The polishing pad may be formed from blown polyurethane (paragraph [0044]). A porous polishing pad facilitates transportation of the electrolytic solution to the wafer (paragraph 0045).

15. The prior art of record is indicative of the level of skill of one of ordinary skill in the art. It would have been obvious at the time the invention was made to have utilized a porous polishing pad as disclosed by Chadda or Emesh in the process of Economikos because transport of the electrolyte solution to the surface of the wafer being processed would have been facilitated.

16. Claims 40 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Economikos et al (US 6,773,570) in view of Chadda (US 7,025,860) or Emesh et al (2002/0108861) as applied to claims 34, 35, 37-39, 41, 43, 44 and 58 above, and further in view of Matsuda et al (US 6,375,823) .

17. Claim 40 additionally recites applying plating voltage after a period of time after the porous contact member is brought into contact with the surface of the seed layer. Claim 42 recites that the porous member and the seed layer are moved relatively before performing plating by flowing current. Economikos is silent as to the sequence of contacting and applying a

voltage. Matsuda discloses that the impregnated pad is brought into tight contact with the seed layer and then a plating current is applied (column 10, lines 26-31). It would have been obvious to have utilized the sequence disclosed by Matsuda in the process of Economikos because plating would not commence until the desired orientation of the parts was obtained.

Response to Arguments

18. Applicant's arguments filed June 22, 2010, have been fully considered but they are not persuasive. At page 8 of the Remarks, applicant argues that in claim 34 the change of state of the plating a voltage and the change of pressing state between the porous contact member and the seed layer occurs during the performance of the plating, while in Economikos the plating and planarization are performed sequentially and the downward force is varied between plating and etching but not during plating. This argument is no convincing. Claim 34 requires that plating be performed while a change of state of the plating voltage that results from intermittence of the plating voltage occurs. As set forth in the grounds of the rejection above, intermittence of the plating voltage is the starting and stopping of the voltage. Claim 34 requires that the recited plating step be performed while this intermittence occurs, i.e., both starting and stopping so that there is at least one interval when plating current is applied and at least one interval when plating current is not applied. Economikos meets this limitation. At page 9, applicant argues that step e) of claim 41 as amended requires the repetition of steps c) and d). For the reasons set forth in the grounds of the rejection, Economikos discloses repetition of steps c) and d). With respect to claim 44 as amended the rejection is based on Economikos for the reasons given in the grounds of rejection. Applicant's arguments with respect to Matsuda are considered to be moot.

Applicant's argument that Chadda or Emesh do not otherwise cure the defects of Economikos with respect to meeting the limitations of independent claims 34 and 41 as well as the respective dependent claims is acknowledged, but not persuasive for the reasons given above. Additionally, applicant arguments with respect to dependent claims 40 and 42 are acknowledged, but not convincing for the reasons given above.

Conclusion

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM T. LEADER whose telephone number is (571) 272-1245. The examiner can normally be reached on Mondays-Thursdays and alternate Fridays, 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick J. Ryan can be reached on 571-272-1292. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/William Leader/
August 27, 2010

/PATRICK RYAN/
Supervisory Patent Examiner, Art Unit 1795